

AMENDMENTS TO THE CLAIMS

- Claim 1 (currently amended): A method for performing a delay lock to generate a second clock according to a first clock and to synchronize the second clock with the first clock, the method comprising:
- executing a plurality of correcting processes, each of which increases or decreases by a respective correction interval a respective delay time between corresponding periods of the first clock and the second clock; and
- prior to the plurality of correcting processes, setting the correction interval to a predetermined initial value;
- wherein a subsequent correction interval for a subsequent correcting process is substantially halfless than a previous correction interval of a previous correcting process.
- Claim 2 (original): The method of claim 1, wherein the correcting process further comprises:
- determining if the first clock and the second clock are synchronized and generating a corresponding comparison result;
- wherein the delay time between the corresponding periods of the first clock and the second clock for the subsequent correcting process is increased or decreased by the subsequent correction interval according to the comparison result.
- Claim 3 (original): The method of claim 2, wherein determining if the corresponding periods of the first

clock and the second clock are synchronized is decided by comparing the time interval between a period of the second clock and a corresponding reference period of the first clock.

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Claim 4 (canceled)

Claim 5 (currently amended): The method of claim 1, wherein the method is used for a delay lock circuit, the delay lock circuit comprising:
a delayer for delaying the ~~second~~first clock in order to change the delay time between the corresponding periods of the second clock and the first clock; wherein when the delay time between the corresponding periods of the first clock and the second clock is increased or decreased by the correction interval, the delayer is used to delay the second clock so that the delay time between the corresponding periods of the first clock and the second clock is modified.

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Claim 6 (original): The method of claim 5, wherein the delayer comprises a plurality of delay units, each of the delay units capable of increasing the delay time between the corresponding periods of the first clock and the second clock by a unit delay time.

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Claim 7 (original): The method of claim 5, wherein the delay lock circuit further comprises a comparator electrically connected to the delayer for determining if the corresponding periods of the first clock and the second clock are synchronized and generating a corresponding comparison result; wherein the delay

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time between the corresponding periods of the first clock and the second clock is increased or decreased by the correction interval according to the comparison result.

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Claim 8 (original): The method of claim 7, wherein the comparator compares the time interval between a period of the first clock and a corresponding reference period of the second clock to generate the comparison result;
10 wherein the period of the first clock corresponding to the period of the second period leads the reference period by a predetermined reference interval.

Claim 9 (original): The method of claim 5, wherein the
15 delay lock circuit further comprises a register to store information about the correction interval.

Claim 10 (original): The method of claim 1 further comprising:
20 terminating the plurality of correcting processes when the correction interval is smaller than a predetermined value.

Claim 11 (currently amended): A delay lock circuit for
25 generating a second clock according to a first clock and synchronizing the first clock and the second clock, the delay lock circuit comprising:
a comparator for determining if corresponding periods
of the first clock and the second clock are
30 synchronized and generating a corresponding comparison signal;
a delayer electrically connected to the comparator for

delaying the ~~second~~first clock so as to change a delay time between the corresponding periods of the first clock and the second clock; and

a controller to control the delay lock circuit;
5 wherein the controller uses the delayer to perform a correcting process to increase or decrease the delay time between the corresponding periods of the first clock and the second clock by a correction interval, wherein a subsequent correction interval of a
10 subsequent correcting process is ~~substantially half~~less than a previous correction interval of a previous correcting process, and the controller terminates the correcting process if the correction interval is smaller than a predetermined value.

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Claim 12 (original): The delay lock circuit of claim 11, wherein the delayer comprises a plurality of delay units, each of the delay units capable of increasing the delay time between the corresponding periods of
20 the first clock and the second clock by a unit delay time.

Claim 13 (original): The delay lock circuit of claim 11, wherein the delay lock circuit further comprises
25 a register to store information about the correction interval.

Claim 14 (original): The delay lock circuit of claim 11, wherein the comparator compares the time interval
30 between a period of the second clock and a corresponding reference period of the first clock to generate the comparison signal, wherein the period of

the first clock corresponding to the period of the second clock leads the reference clock by a predetermined reference interval.

5 Claim 15 (canceled)

Claim 16 (new): A method for performing a delay lock to generate a second clock according to a first clock and to synchronize the second clock with the first
10 clock, the method comprising:

executing a plurality of correcting processes, each of which increases or decreases by a respective correction interval a respective delay time between corresponding periods of the first clock
15 and the second clock; and

terminating the plurality of correcting processes when the correction interval is smaller than a predetermined value;

wherein a subsequent correction interval for a
20 subsequent correcting process is less than a previous correction interval of a previous correcting process.

Claim 17 (new): The method of claim 16, wherein the correcting process further comprises:

25 determining if the first clock and the second clock are synchronized and generating a corresponding comparison result;

wherein the delay time between the corresponding periods of the first clock and the second clock for
30 the subsequent correcting process is increased or decreased by the subsequent correction interval according to the comparison result.

Claim 18 (new): The method of claim 17, wherein
determining if the corresponding periods of the first
clock and the second clock are synchronized is decided
5 by comparing the time interval between a period of the
second clock and a corresponding reference period of
the first clock.

Claim 19 (new): The method of claim 17 further
10 comprising:
prior to the plurality of correcting processes,
setting the correction interval to a
predetermined initial value.

15 Claim 20 (new): The method of claim 17, wherein the
method is used for a delay lock circuit, the delay lock
circuit comprising:
a delayer for delaying the first clock in order to
change the delay time between the corresponding
20 periods of the second clock and the first clock;
wherein when the delay time between the corresponding
periods of the first clock and the second clock is
increased or decreased by the correction interval, the
delayer is used to delay the second clock so that the
25 delay time between the corresponding periods of the
first clock and the second clock is modified.

Claim 21 (new): The method of claim 20, wherein the
delayer comprises a plurality of delay units, each of
30 the delay units capable of increasing the delay time
between the corresponding periods of the first clock
and the second clock by a unit delay time.

Claim 22 (new): The method of claim 20, wherein the delay lock circuit further comprises a comparator electrically connected to the delayer for determining
5 if the corresponding periods of the first clock and the second clock are synchronized and generating a corresponding comparison result; wherein the delay time between the corresponding periods of the first clock and the second clock is increased or decreased
10 by the correction interval according to the comparison result.

Claim 23 (new): The method of claim 22, wherein the comparator compares the time interval between a period
15 of the first clock and a corresponding reference period of the second clock to generate the comparison result; wherein the period of the first clock corresponding to the period of the second period leads the reference period by a predetermined reference interval.

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Claim 24 (new): The method of claim 20, wherein the delay lock circuit further comprises a register to store information about the correction interval.